

ABSTRACT OF THE DISCLOSURE

Memory array areas, each including a plurality of bit lines provided along a first direction, a plurality of word lines provided along a second direction orthogonal to the first direction, and a plurality of memory cells provided in association with portions where the plurality of bit lines and the plurality of word-lines intersect, respectively, are provided in plural form in the first direction and are disposed alternately relative to sense amplifier areas. First common input/output lines connected through bit lines and first selection circuits associated with such sense amplifier areas are provided. Second common input/output lines connected through the plurality of first common input/output lines and second selection circuits corresponding to a plurality of memory arrays disposed along the first direction are provided. Each of the second common input/output lines is extended to form a signal transfer channel for transferring a signal read from each memory cell and a signal written therein.